A high-speed imager with low-power PTC-inspired column-multiplexed readout

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Abstract

We fabricated a large stitched image sensor with a low-noise high speed readout. The 12b ADC employs a two-step operation that enables an improved tradeoff between read noise and speed, by choosing a smaller LSB in dark regions and relaxing read noise in the light regions. The first stage increases the speed by using eight parallel stages per pixel column while also converting the two MSBs. A highly efficient 10 bit SAR ADC is used as the second stage. The ADC achieves an effective row rate of 1 Mrows/s and a read noise of 270 µV in dark. The 1 Mpix version of the sensor consumes 741 mW at 1000 fps which results in a imager power efficiency of 698 pJ/pix at 12 bit resolution.

Introduction

When high speed and low power operation are required in image sensors, the impractical long and narrow form factor of column-parallel ADCs limits the flexibility for optimization. Hence, the ADCs used in high-speed image sensors are often not as efficient as the state of the art ADCs. More so, image sensor ADCs are often conceptually overdesigned, achieving low noise over the complete input range. In reality, low noise is only required for the dark end of the input range and not for stronger input signals, due to the photon shot noise properties [1].

Furthermore, when the pixel area is large, also column settling time impedes high-speed operation [2]. Indeed, despite of high-speed analog-to-digital conversion, column lines need time to settle. Also this complicates the development of efficient, high-speed readout techniques.

This work addresses the above items, and presents a large, high-speed image sensor with low-noise, high-speed readout.

Column settling

The targets for the readout have been set with a large pixel array in mind, with a size of up to 4096 rows. For these large pixel arrays, especially in combination with large pixels, column line settling also becomes a speed bottle neck. To alleviate this, eight parallel column lines per pixel column have been selecting, allowing for sufficient column line settling time with up to 12 bit settling. These column outputs run completely synchronous to avoid any type of cross-talk which would complicate settling, as could be achieved with time-interleaved column lines. This means that eight rows are measured at the same time. It also implies that the array provides eight parallel outputs must be sampled and converted at the same time, within a single pixel column, in order to give the column lines sufficient time to settle for the next pixel row block. This in turns complicates the readout design as the effective pitch for the ADC becomes $1/8^{th}$ of the pixel pitch.

High speed readout

To address the above, the following readout architecture has been conceived. The readout core consists of a two-step ADC (Figure 1), which alleviates speed limitations and enables design flexibility. The first stage is implemented as a two-phase CDS amplifier with a programmable gain step (4x, 2x or 1x). While the amplifier samples, amplifies the column line output and settles, the gain is automatically toggled progressively from high to low in order to apply the largest possible gain to the pixel output signal that fits the input range of the second stage. As a result, the first stage performs automatically and during the amplification phase a two bit MSB conversion. The conditionally amplified signal is then provided to a 10 bit ADC. Consequentially, the overall readout chain has an LSB size depending on the input level and matched to the photon shot noise behavior. The larger the input signal, the higher the signal shot noise, the lower the amplifier gain, and the larger the ADC LSB. The timings for this two-step ADC are exemplified in Figure 2.

The operation of this first stage is completely synchronous to the pixel operation and the outputs presented by the column lines. Eight parallel amplifiers per column have been used, each converting the two bit simultaneously.

The 2^{nd} stage is implemented as a fast, highly-efficient charge-sharing 10 bit SAR ADC [3]. This ADC is shared per two pixel columns which allows for a more relaxed form factor as required for SAR ADCs and enables very low-power, high-speed conversions. A pipe-lined operation allows the first step to start with the next readout cycle, while the SAR ADC sequentially converts the 16 voltages (8 amplifiers x 2 pixel columns).

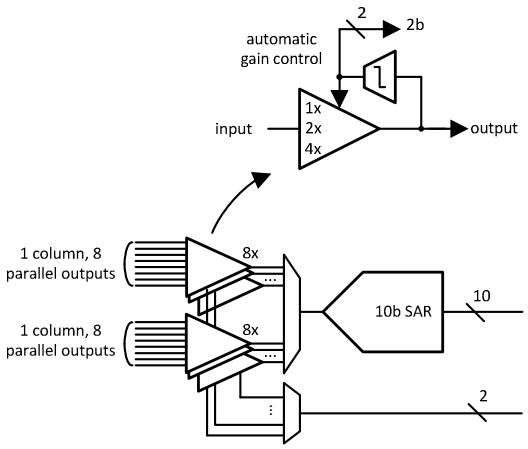
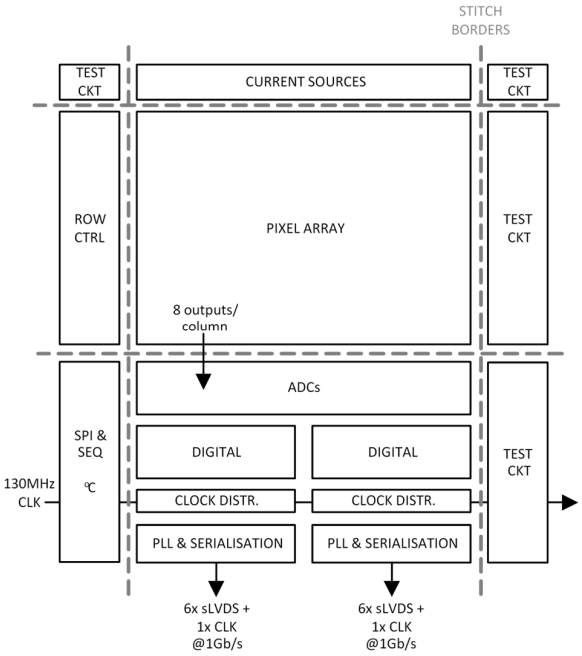


Figure 1: Readout ADC architecture with 8 parallel outputs per column and 2-step PTC-inspired ADC.



Sensor implementation

Using this readout approach, a 1024x1024 image sensor has been developed using imec's 130 nm CIS process, with 14 µm pixels. The architecture is depicted in Figure 3. The design is stitch-compatible in blocks of 1024x1024 pixels up to 4096x4096 pixels.

The device accepts a single 130 MHz clock, distributed across the chip. This allows clock propagation across long distances in stitched designs. Two local on-chip PLLs per stitch block and per 6 output channels generate the high-speed clocks required. To reduce power as much as possible for large stitched designs, sLVDS is used and each output channel consumes about 5 mW at 1.05 Gb/s.

With the current pixel pitch, thanks to the parallelism, the effective ADC pitch is 1.8 µm, though the implementation is heavily facilitated.

The overall sensor speed is limited by the required bit depth as well as the digital output data rate. To increase frame rate, the overall sensor output resolution can be reduced from 12 bit to 8 bit or 6 bit for which the LSB and readout input range can be arbitrarily chosen. This leads to an increase of the frame rate to 1424 fps (8 bit mode) and 2000 fps (6 bit mode). A flexible ROI is also incorporated into the sensor for even higher readout speed. The minimum ROI is eight rows tall.

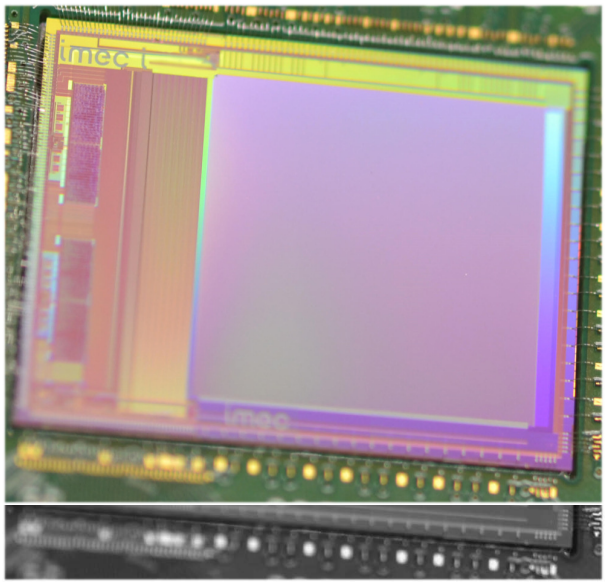


Figure 4: Chip photograph of the sensor bond wired to the board.

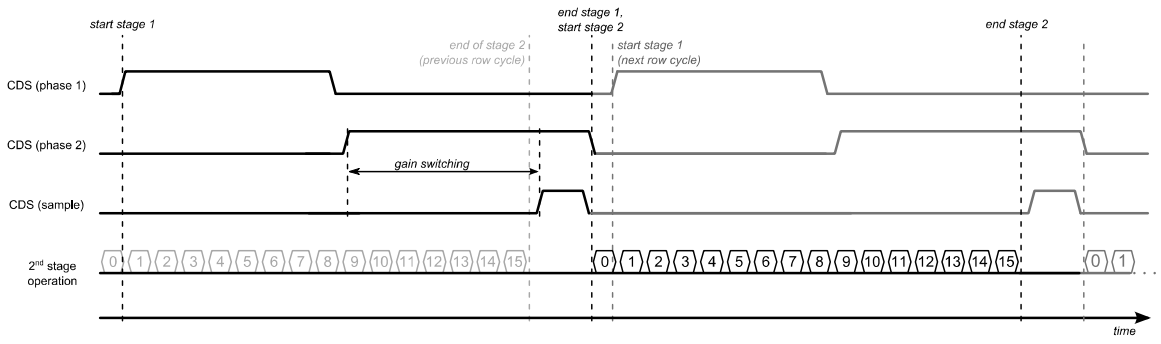


Figure 2: The timings used in the two-step ADC.

Measurement results

A photograph of the sensor on our test PCB is shown in Figure 4. The die measures 18x24 mm^2.

In 12b mode, the sensor achieves 50dB SNR, while consuming merely 741mW at its maximum rate of 1,000 fps at full frame operation.

Figure 5 shows a typical measured DNL/INL plot for the 10 bit SAR ADC in the sensor which results in a ENOB (Effective Number of Bits) of about 9 bit. This has been characterized with a test input towards the ADC input.

With a similar analog test input voltage connected toward the input of the whole read chain, a similar characterization has been done. The read noise over the full input range is depicted in Figure 6. Below ~1024 DN (the first quarter of the scale), the first stage uses a 4x gain and the lowest read noise is found here to be 270 μV_{rms} (~1LSB), referred to the pixel input. Between ~1024 DN and ~2048 DN (the second quarter of the scale), the amplifier uses 2x gain and hence a larger read noise is found (428 μV_{rms}), since the ADC noise is less suppressed, and the LSB step is larger. Above 2048 DN (last half of the scale), the amplifier uses 1x gain and the largest read noise is found (750 μV_{rms}). This scale has been designed to keep the readout noise well be below the photon shot noise floor. A raw picture taken with the sensor is shown in Figure 7.

Figure 8 shows the measured PTC (Photon Transfer Curve). The conversion gain and dark noise, resolved from the PTC are 15.8 µV/e- and 75 e- respectively, with dark noise limited by the 3T pixel required by the application.

Given this effective performance, the two-step ADC efficiency is about 75 fJ/conversion step. The effective imager efficiency is 698 pJ/pixel, enabled by the highly efficient readout and digital sub-LVDS transmitters, confirms the viability of the proposed techniques.

While the stitched sensor presented here measures only 1024x1024 pixels, successful versions have been fabricated with up to 16 Mpix, demonstrating the viability of the techniques, and showing that all performance (speed, power consumption) scale linearly and accordingly.

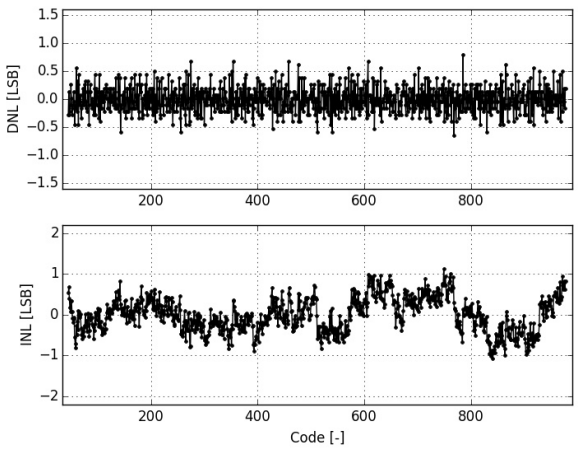


Figure 5: INL/DNL of the 10b SAR ADC.

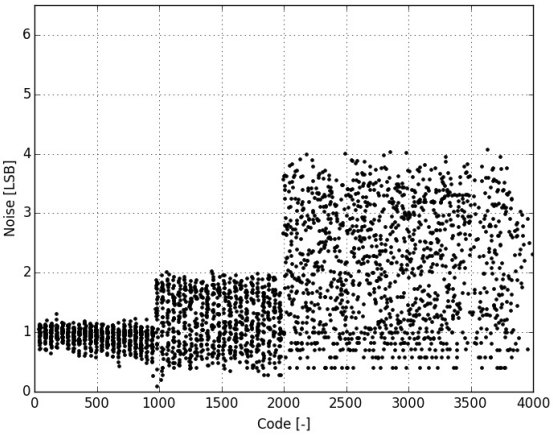


Figure 6: Input-referred read noise (in LSB) as a function of input range: the dark portion of the input range has a smaller LSB than the brighter portion of the range.

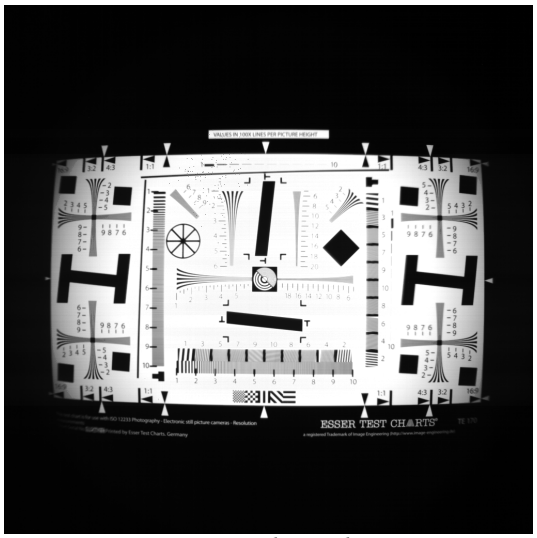


Figure 7: Raw picture taken with imager.

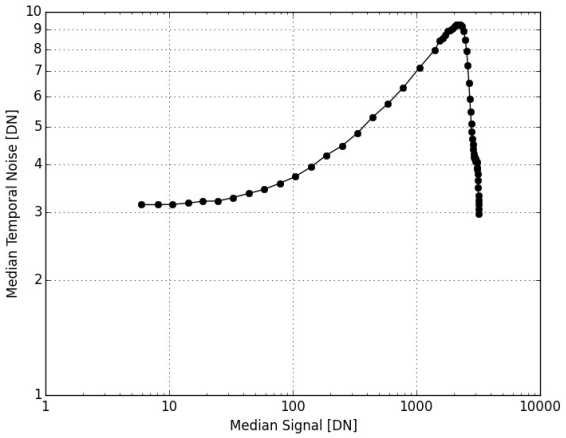


Figure 8: Photon transfer curve.

Conclusions

This work demonstrates how multiple parallel column lines can alleviate the column line settling issues in large image sensors, while parallelized readout schemes and two-step PTC-inspired ADCs allow to achieve a very low-power sensor design.

While the work presented here is a 1024x1024 stitched image sensor, successful version of the sensor have been fabricated with stitching up to 16 Mpix, where the concept proves to scale and be compatible with very large areas.

Table 1: sensor performance overview

Specification	This work 1k-1k
Array size	1024x1024
Pixel size	14 µm
Full well capacity	100 ke-
ADC readout noise	271 µV
Frame rate	2000 fps @6b 1,424 fps @8b 1,000 fps @12b
Power consumption	741 mW @12b, 1000 fps
Imager power efficiency	698 pJ/pix @12b
sLVDS channels	12x 1.05 Gb/s
Supply voltages	3.3V, 2.5V & 1.2V
Technology	130 nm CMOS CIS

References

[1] M. F. Snoeij, A. J. P. Theuwissen, K. A. A. Makinwa, and J. H. Huijsing, "Multiple-Ramp Column-Parallel ADC Architectures for CMOS Image Sensors", IEEE J. Solid-State Circuits, vol. 42, no. 12, pp. 2968−2977, Dec. 2007.

[2] G. Meynants, G. Lepage, J. Bogaerts, G. Vanhorebeek and X. Wang, "Limitations to the frame rate of high speed image sensors", in Proc. of 2009 Int. Image Sensor Workshop (IISW), Paper 37, June 2009

[3] J. Craninckx and G. Van der Plas, "A 65fJ/Conversion-Step 0-to-50MS/s 0-to-0.7mW 9bCharge-Sharing SAR ADC in 90nm Digital CMOS", in Int. Solid-State Circuits Conf., pp. 246−247, Feb. 2007